Amendments to the Specification:

Please replace paragraph beginning on page 2, line 14 with the following amended paragraph:

However, the selective allocation of data to disparate memory devices, depending on either the nature or the intended application of the data, tends to preclude a coherent or uniform approach to the manner in which data is managed in a system. To wit: techniques that are appropriate to the management of transitory data stored in semiconductor SRAM (static random access memory) are likely to be inapposite to the management of persistent data stored in CMOS (complementary metal oxide semiconductor) ROM (read only memory). Furthermore, although a number of emerging memory technologies have appeared that promise performance capabilities that may enable the storage of both persistent data and dynamic data, there does not yet exist a comprehensive approach to the management of disparate data types in a unified memory system. (In this regard, a "unified" memory system may be considered to be one that exhibits a combination of properties, such as ~~nonvolatibity~~ nonvolatility, nondestructability, cell density and access speeds, that had not heretofore been available in a single memory type.)

Please replace paragraph beginning on page 5, line 12 with the following amended paragraph:

As seen in FIG. 1, memory level 101 comprises a number of memory segments, 111, 112, and 113. As will be made clear below, memory segments 111, 112, and 113 in memory level [[10]] 101, may be used to store data fragments. Each memory segment comprises a respective number of discrete memory locations that comprise a predetermined number of memory cells (not shown). In some embodiments, the number of memory locations that constitute a segment may be fixed to a predetermined number, such as, 10K bytes (where 1K = 1024); but such is not necessarily the case. In general, data fragment segments 111, 112, 113, etc. may be varying sizes.

Please replace paragraph beginning on page 7, line 13 with the following amended paragraph:

Note that in the embodiment of FIG. 1, data fragments reside in respective data fragment segments that occupy ascending positions in memory level 101. Because the data unit header that is associated with a respective [[a]] data fragment segment is positioned in memory level 101 in proximity to the respectively associated data fragment segment, data unit headers and data fragment segments occupy alternating consecutively ascending positions in memory level 101,

beginning at, or in proximity to, memory management boundary 110. In the embodiment of FIG. 1, sequence tables occupy descending positions in level 101, beginning at, or near, memory management boundary 110.

Please replace paragraph beginning on page 7, line 25 with the following amended paragraph:

With continuing reference to FIG. 1, dual-level segmented memory [[110]] 10 is seen to also include memory level 102. Memory level 102 comprises memory segments that reside logically above memory management boundary 110. Because memory level 101 comprises memory segments that reside below memory management boundary 110, level 101 may be considered the lower memory level, and level 102 may be considered the upper memory level. As seen in FIG. 1, upper memory level 102 comprises a plurality of data unit segments 141, 142 and 142 and comprises a plurality of corresponding object pointers 151, 152 and 153. Each of the object pointers points to a respective associated data unit segment. That is, each of the object pointers contains an address (generally, a starting address) of a respective associated data unit. Object pointer 151 points to data unit segment 141, object pointer 152 to data unit segment 142, and so forth. To promote simplicity, only three sets of object pointers and associated data unit segments are explicitly depicted in FIG. 1. However, the scope of the present invention is not constrained by a particular number of object pointers and data unit segments. As a practical matter, only the number of memory locations available in level 102 and the combined sizes of the data unit segments limit the number of data unit segments that may be stored by second memory level 102.